Most significant scientific results in 2018
Department of design and diagnostics of digital systems
(1000 characters maximum + 1 figure)

2.3.1. Fundamental research

Result name: Enhancement of digital circuit reliability on the random logic and RAM level using redundancy elements
Authors: Dr. Štefan Krištofík, Dr. Marcel Baláž, Dr. Peter Malík.
Project type and number: VEGA 2/0192/15
Annotation:
This research is motivated by the increasing failure rates of digital circuits caused by continuous reduction of semiconductor manufacturing processes. It is necessary to keep high reliability of components, especially in critical domains such as transportation, health care or space missions. The research goal is to increase the long-term reliability of these circuits, more precisely on the logic level [1] and RAM memory level [2] in the embedded systems-on-chip. Both proposed solutions use the method of adding redundancy elements.
A new architecture using reconfigurable logic blocks for random logic is proposed in [1]. A new architecture for better effectiveness of detection and processing of fault information in RAMs is proposed in [2]. Experimental results show that both solutions have positive impact on the reliability of the backed-up part of the system with random logic (Figure 1) [1], and RAM memories [2] by up to 5 %, respectively. Apart from reliability, both proposed solutions also focused on the other important task, which is to minimize the amount of additional chip area caused by adding redundancy. This additional area was successfully kept at low levels.

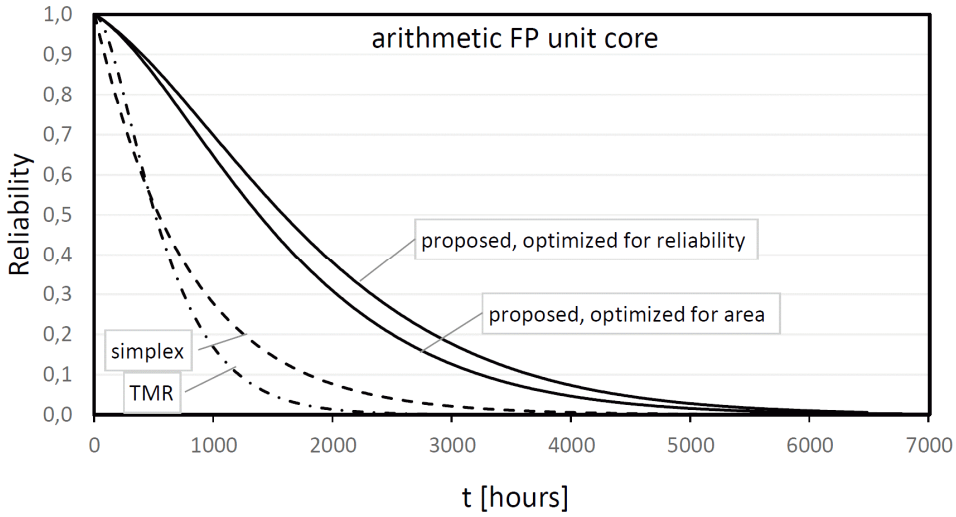

Figure 1. Reliability of the backed-up part of the system with random logic [1].

Main scientometric research outputs:

1. KRIŠTOFÍK, Štefan - BALÁŽ, Marcel - MALÍK, Peter. Hardware redundancy architecture based on reconfigurable logic blocks with persistent high reliability improvement. In Microelectronics reliability, 2018, vol. 86, p. 38-53. ISSN 0026-2714. Type: **ADCA**.
2. KRIŠTOFÍK, Štefan - MALÍK, Peter. Enhancement of fault collection for embedded RAM redundancy analysis considering intersection and orphan faults. In Integration: the VLSI Journal, 2018, vol. 62, p. 190-204. ISSN 0167-9260. Type: **ADCA**.